0956956 - 090904

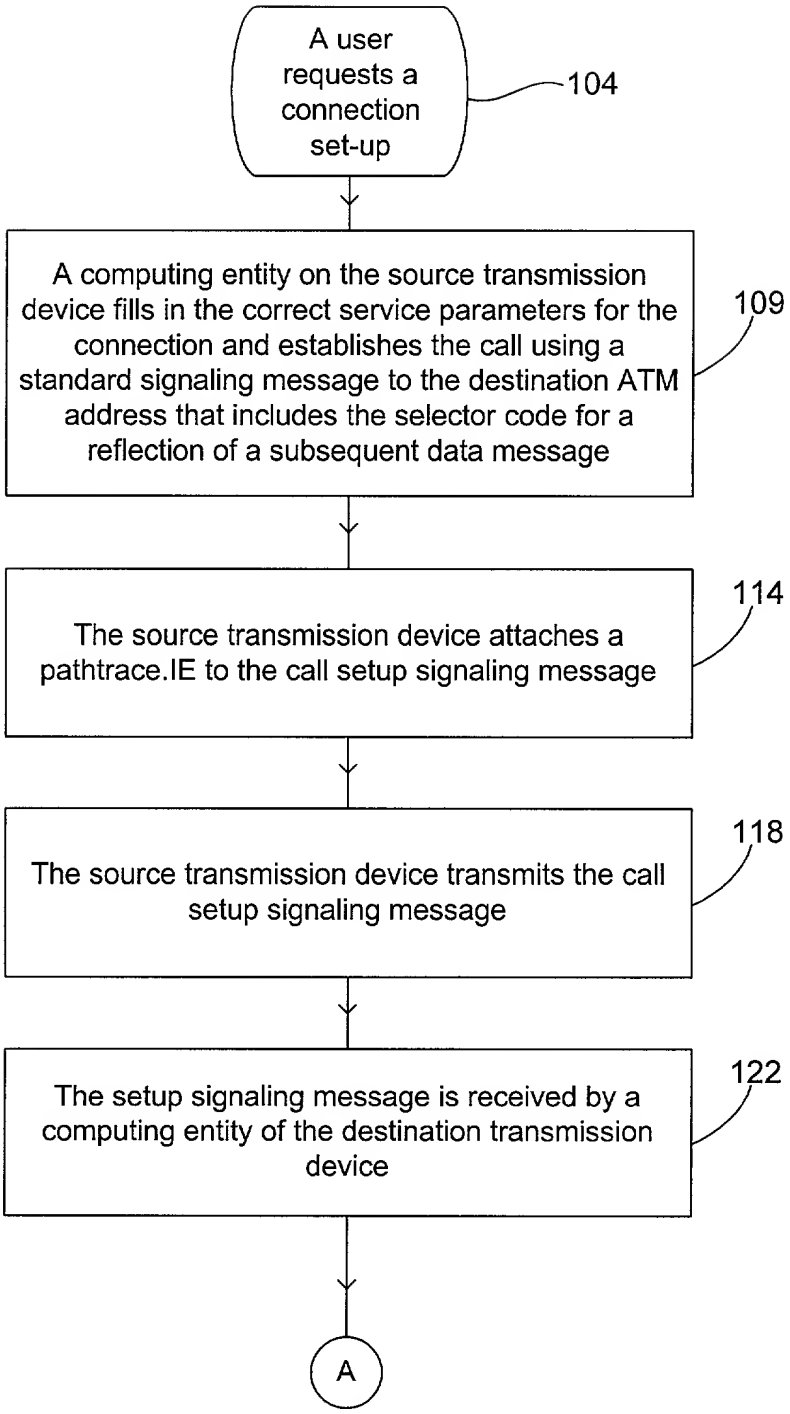

Figure 1a

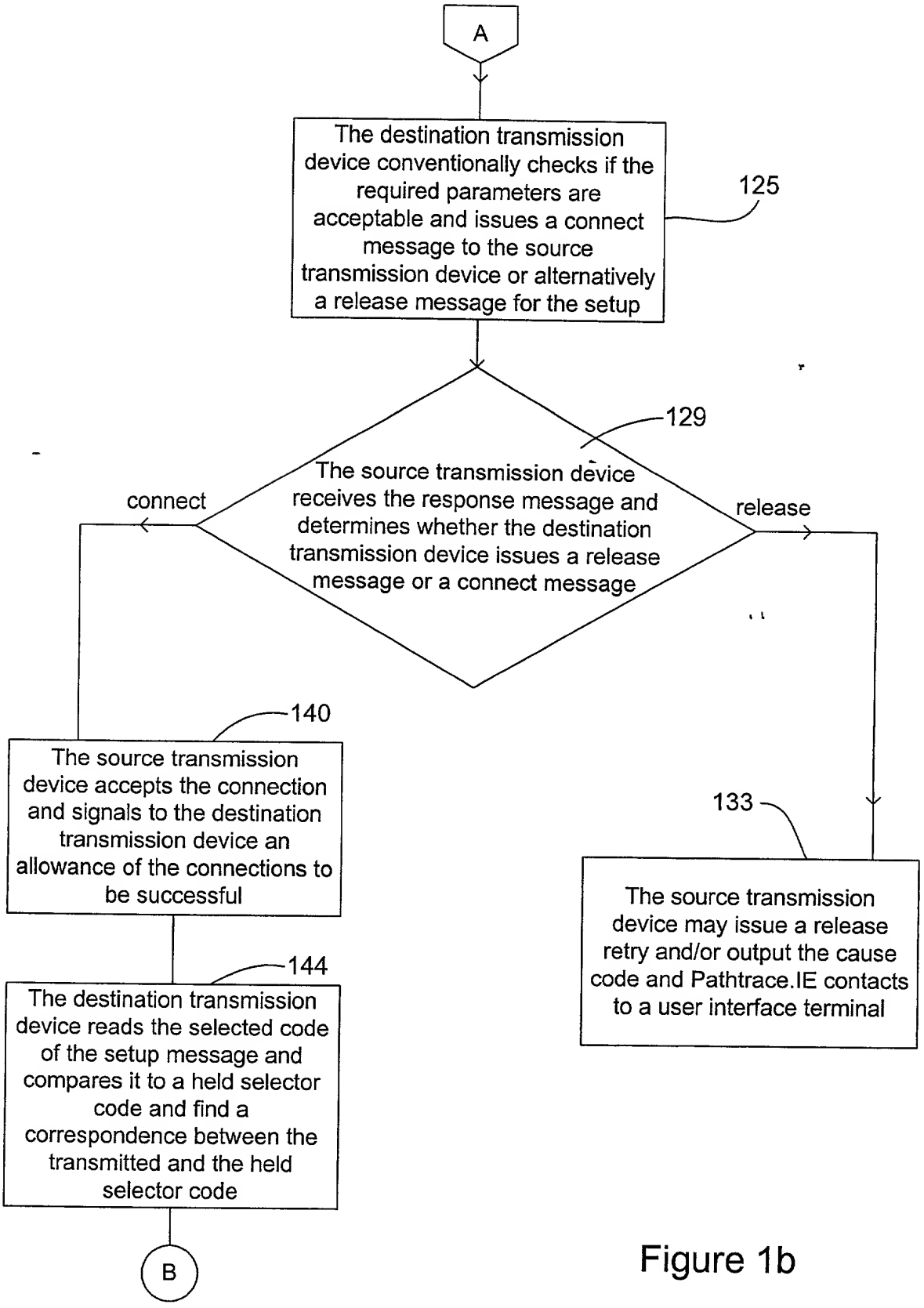
A
The destination transmission device conventionally checks if the required parameters are acceptable and issues a connect message to the source transmission device or alternatively a release message for the setup
125
129
The source transmission device receives the response message and determines whether the destination transmission device issues a release message or a connect message
connect
release
140
The source transmission device accepts the connection and signals to the destination transmission device an allowance of the connections to be successful
133
The source transmission device may issue a release retry and/or output the cause code and Pathtrace.IE contacts to a user interface terminal
144
The destination transmission device reads the selected code of the setup message and compares it to a held selector code and find a correspondence between the transmitted and the held selector code
B

Figure 1b

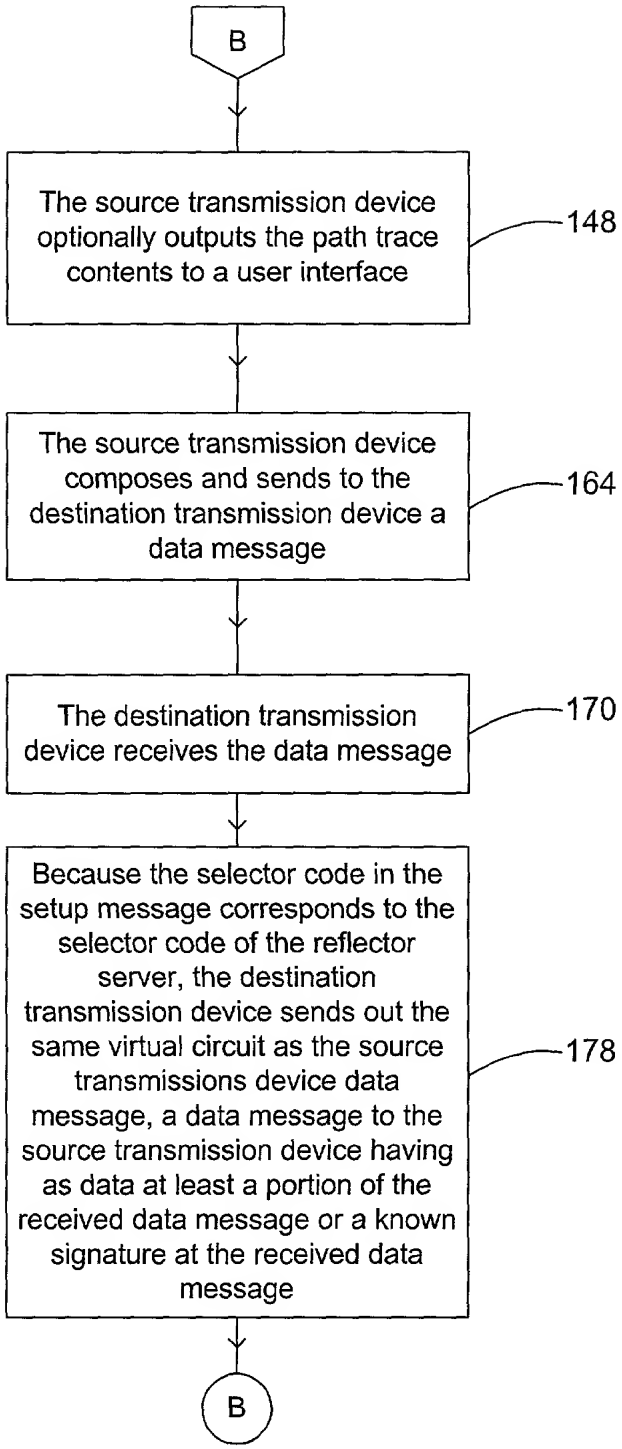
B
The source transmission device optionally outputs the path trace contents to a user interface
148
The source transmission device composes and sends to the destination transmission device a data message
164
The destination transmission device receives the data message
170
Because the selector code in the setup message corresponds to the selector code of the reflector server, the destination transmission device sends out the same virtual circuit as the source transmissions device data message, a data message to the source transmission device having as data at least a portion of the received data message or a known signature at the received data message
178
B

Figure 1c

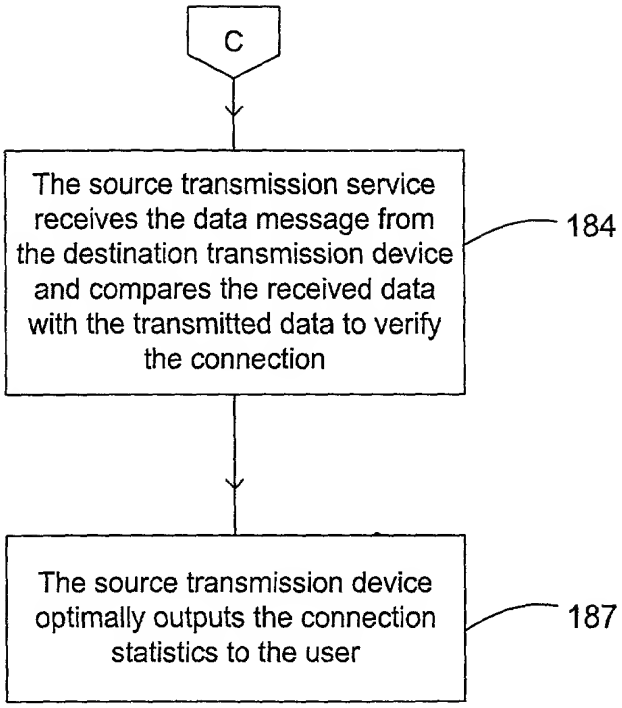
C
The source transmission service receives the data message from the destination transmission device and compares the received data with the transmitted data to verify the connection
184
The source transmission device optimally outputs the connection statistics to the user
187

Figure 1d

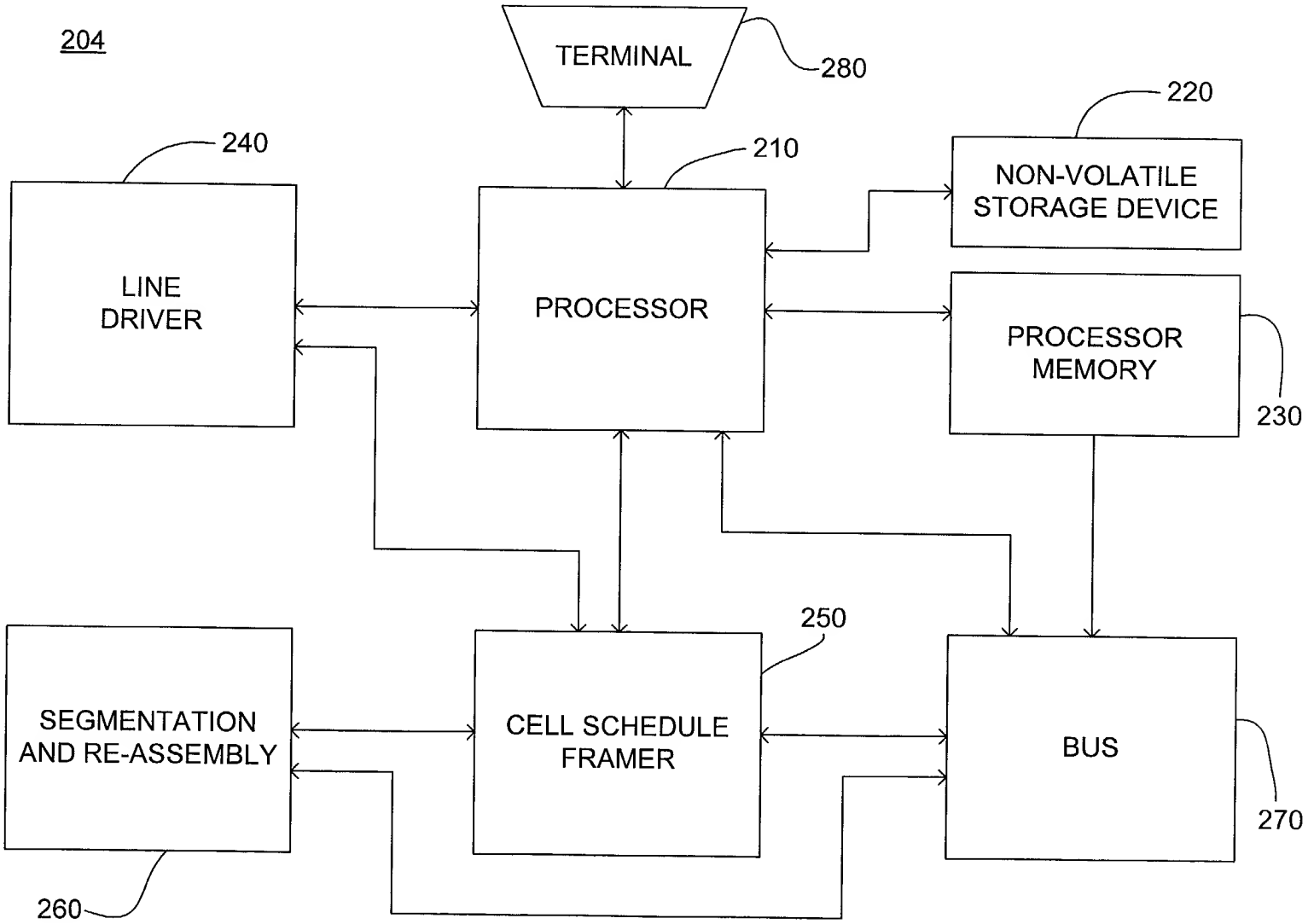
204
TERMINAL
280
220
240
210
NON-VOLATILE STORAGE DEVICE
LINE DRIVER
PROCESSOR
PROCESSOR MEMORY
230
250
SEGMENTATION AND RE-ASSEMBLY
CELL SCHEDULE FRAMER
BUS
270
260

Figure 2

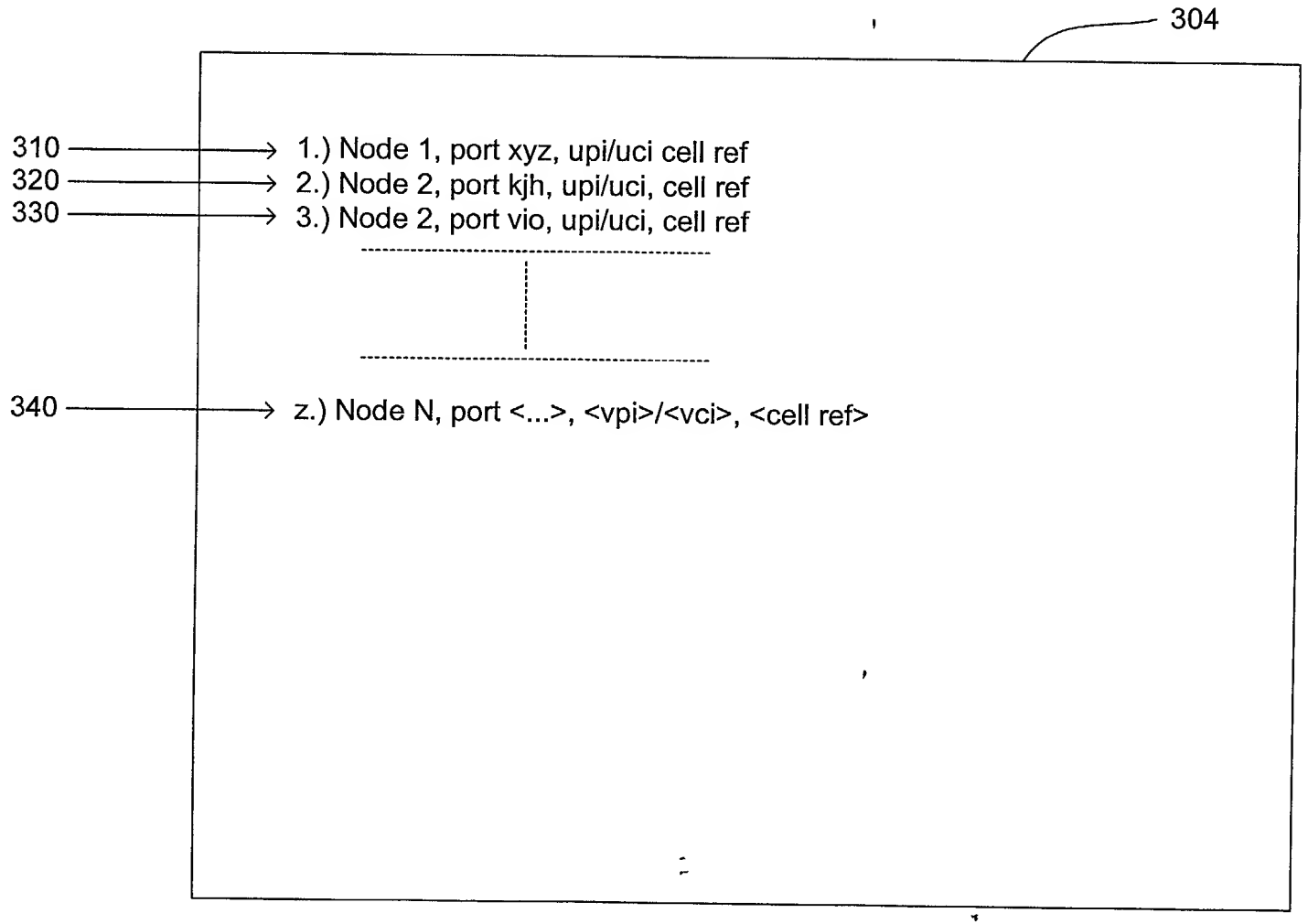
304
310
320
330
1.) Node 1, port xyz, upi/uci cell ref
2.) Node 2, port kjh, upi/uci, cell ref
3.) Node 2, port vio, upi/uci, cell ref
340
z.) Node N, port <...>, <vpi>/<vci>, <cell ref>

Figure 3